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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,128	03/25/2002	Chao-Hu Liang	NAUP0385USA	5968

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/063,128	LIANG ET AL.
	Examiner	Art Unit
	Anh D. Mai	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1-17 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in specification, Paper No. 1, filed March 25, 2002. In that paper, applicant has stated "contaminants adhering to the semiconductor wafer 100 **are removed**" (see [0025]); "the present invention shows marked improvement in **preventing the occurrence of particles and defects** of various shapes and sizes" (see [0030]), and this statement indicates that the invention is different from what is defined in the claim(s) because claim 2 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (line 2) and "which **utilizes the particles** on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film" (lines 10-12).

Note that, "preventing the occurrence of particles and defects" is achieved by the cleaning process, not the formation of the α-Si.

With respect to claim 4, claim recites: "wherein the wet etching process comprises a megasonic scrubbing process, a SC-1 cleaning process and a SC-2 cleaning process".

However, the specification discloses: "After removing the photoresist layer 112, a wet etching process is performed. Usually, a megasonic scrubbing process is first performed. By

utilizing vibration of the megasonic scrubbing, contaminants, adhering to the semiconductor wafer 100 **are removed**". (See [0025]).

As disclosed, the megasonic scrubbing is **not** part of the wet etching but it is part of the cleaning process. While the wet etch is to remove the oxide formed in area 104. (See Fig. 10, also see claim 13).

2. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (line 2) and "which **utilizes the particles** on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film" (lines 10-12).

Limitations of claim 1 are inconsistent with the aim of the present invention, e.g. preventing the occurrence of particles and defects.

The specification clearly states: "Consequently, grains growing via small and large particles adhering on the surface of the semiconductor wafer during the crystallization, and which thus generate various unexpected needle-like particles, **can be avoided**". (See [0030]).

With respect to claim 9, the "avoid formation of particles and defects" are the result of the cleaning process, not the deposition process.

The indefiniteness of claims 5 and 17, have prevented these claims from being properly examined for merits.

Claim Objections

3. Claims 1, 8, 9 and 16 are objected to because of the following informalities:

Claim 1 recites: "performing a two-step polysilicon deposition process", the correct terminology should be "performing a two-step **silicon** deposition process" because layer 116a is **amorphous** silicon, not polysilicon.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004).

With respect to claim 1, as best understood by the examiner, Balasubramanian teaches a method for making a polysilicon film on a semiconductor wafer, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (16) deposition process utilizing a low temperature; and

a second step polysilicon (18) deposition process utilizing a high temperature;

wherein the first step amorphous silicon (16) deposition process is used to avoid nucleation of the polysilicon film growth, so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film. (See Fig. 1, col. 1-12).

With respect to claim 7, the polysilicon layer (18) of Balasubramanian is deposited at the temperature that includes the claimed range.

With respect to claim 8, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian includes single wafer type LPCVD equipment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 as applied to claim 1 above, and further in view of Yu et al. (U.S. Patent No. 6,225,167).

With respect to claim 2, Balasubramanian teaches a method of making a polysilicon film on a semiconductor wafer including performing a two-step silicon deposition process.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of disclosing the process performing before the two-step silicon deposition process.

However, Yu teaches the process performing prior to making conductive gate electrodes including: at least one photolithography process, one wet etching process, one photoresist stripping process, one wet cleaning process and one thermal oxidation process are performed on the surface of the semiconductor wafer (200).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to before performing the two-step silicon deposition process of Balasubramanian performing the processes as taught by Yu to form the gate oxide for the silicon gate electrodes.

With respect to claim 3, as best understood by the examiner, the wet etching process of Yu comprises a buffer oxide etchant (BOE) etching process and followed by a SC-1 cleaning process.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004.

Balasubramanian teaches the first step amorphous (16) is deposited at a temperature range that overlaps the claimed range and at a thickness of about 400 Å.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of explicitly forming a thinner amorphous layer. Note that, the claimed thickness does not appear to be critical.

Therefore, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum thickness of the amorphous silicon layer in the formation of the conductive gate electrodes. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

7. Claims 9-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '167 in view of Balasubramanian '004.

Yu teaches a method for forming a polysilicon film on a semiconductor wafer, a surface of the semiconductor wafer comprising a first gate oxide area (40) and a second gate oxide area (50), substantially as claimed including:

forming a first gate oxide layer (20) on the surface of the semiconductor wafer (10);

performing a photolithography process and an etching process to remove the first gate oxide layer (20) on the surface of the second gate oxide area (50);

performing a cleaning process; and performing a conductive gate electrodes deposition process covering the first gate oxide area (40) and the second gate oxide area (50) to form MOS transistors. (See Fig. 1a-d, col. 1-10).

Thus, Yu is shown to teach all the features of the claim with the exception of explicitly disclosing process of making the conductive gate electrodes.

However, Balasubramanian teaches a process of forming conductive gate electrodes covering gate oxide including:

performing a two-step silicon deposition process to form a polysilicon layer (18), the polysilicon layer (18) covering the gate oxide layer (14);

wherein the two-step silicon deposition process comprises a first step low temperature amorphous silicon (16) deposition process to avoid formation of particles and defects during the formation of the polysilicon layer (18), and a second step high temperature polysilicon (18) deposition process. (See Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the conductive gate electrodes of Yu using the two-step silicon deposition process as taught by Balasubramanian to form a low impurity diffusion polysilicon layer within an integrated circuit. (See col. 3, lines 6-8).

With respect to claim 10, the etching process of Yu is a wet etching process.

With respect to claim 11, the wet etching process of Yu utilizes a buffer oxide etchant (BOE).

With respect to claim 12, the cleaning process of Yu is a wet cleaning process.

With respect to claims 14 and 15, the temperature ranges of the first step low temperature of amorphous silicon (16) deposition process and second step high temperature polysilicon (18) deposition process of Balasubramanian overlaps the claimed range.

With respect to claim 16, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian includes single wafer type LPCVD equipment.

8. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and Yu '167 as applied to claims 2 and 9 above, and further in view of Hayakawa (U.S. Patent No. 5,779,520).

As best understood by the examiner, Balasubramanian '004 and Yu '167 teach a wet cleaning process utilizing RCA clean. Note that RCA cleaning comprises SC-1 and SC-2.

Thus, Balasubramanian '004 and Yu '167 are shown to teach all the features of the claim with the exception of further utilizing megasonic scrubbing.

However, Hayakawa teaches: cleaning is more effective with physical scrubbing including megasonic scrubbing. (See col. 2, lines 56-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to combine RCA cleaning of Yu with megasonic scrubbing as taught by Hayakawa for utmost effective in removing contaminants.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 18, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800